UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,273	01/14/2004	Richard Alan Hamersley	1001-0242	4547

22120 7590 02/22/2007
ZAGORIN O'BRIEN GRAHAM LLP
7600B NORTH CAPITAL OF TEXAS HIGHWAY
SUITE 350
AUSTIN, TX 78731

EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,273	HAMERSLEY, RICHARD ALAN	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-17,19-29,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,8-11,19-25 and 31* is/are allowed.

6)☐ Claim(s) *7, 12-17, 26-29 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This final office action is in response to amendments filed on 11/20/06.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7, 12-17, 26-29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Cooper, US Patent Application Publication no. 2003/0120961.

Regarding claim 7, Cooper discloses a method of operating a computer system comprising:

determining if any performance state data stored in the computer system in a first area of memory specifying performance states for a plurality of processors and is associated with a processor being utilized in the computer system [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

if a portion of the performance state data is found to be associated with the processor being utilized in the computer system, copying the portion of the performance state data into a second area of memory [copy processor performance table to local table, Figure 4 and paragraph 0045].

Cooper further discloses copying default performance state table data into local memory when no match is found [Figure 4 and paragraph 0045].

Regarding claim 12, Cooper discloses a method of operating a computer system comprising:

determining if any performance state data stored in the computer system specifying performance states for a plurality of processors is associated with a processor being utilized in the computer system [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

generating performance state data if none of the performance state data is associated with the processor being utilized in the computer system [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 13, Cooper further discloses copying default performance state table data into local memory when no match is found [Figure 4 and paragraph 0045].

Regarding claim 14, Cooper further discloses that the generating the performance state data further comprises generating performance state information including a plurality of frequency values and a fixed voltage value [paragraph 0038].

Regarding claim 15, Cooper further discloses that an upper limit of frequency of the frequency values is determined according to providing an indication of maximum frequency in the processor [paragraph 0038].

Regarding claim 16, Cooper further discloses that the plurality of frequency values are spread approximately evenly between a lower limit and the upper limit [paragraph 0038].

Regarding claim 17, Cooper discloses a computer program product stored on computer readable medium operable in a computer system to:

determine whether a match exists between a processor being utilized in the computer system and performance state information stored in a first area of memory [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

if a match exists, copying matching performance state information into a second area of memory, wherein the first area of memory is a memory segment utilized during power on self test (POST) processing by basic input output system (BIOS) and wherein the second area of memory is a runtime memory segment of BIOS [copy processor performance table to local table, Figure 4 and paragraphs 0040, 0044 and 0045].

Cooper further discloses generating a performance state data after no match is found to exist between any of the performance state data and the processor being utilized in the computer system [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 26, Cooper discloses a computer program product stored on computer readable medium operable in a computer system to:

determine whether a match exists between a processor being utilized in the computer system and performance state information for a plurality of processors [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

generate performance state data after no match is found to exist [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 27, Cooper further discloses that the generating the performance state data further comprises generating performance state information including a plurality of frequency values and a fixed voltage value [paragraph 0038].

Regarding claim 28, Cooper further discloses that an upper limit of frequency of the frequency values is determined according to providing an indication of maximum frequency in the processor [paragraph 0038].

Regarding claim 29, Cooper further discloses that the plurality of frequency values are spread approximately evenly between a lower limit and the upper limit [paragraph 0038].

Regarding claim 32, Cooper discloses an apparatus comprising:

means for determining if performance state data stored in the computer system specifying performance states for a plurality of processors is associated with a processor being utilized in the computer system [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

means for generating performance state data if none of the performance state data is associated with the processor being utilized in the computer system [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Allowable Subject Matter

Claims 1-5, 8-11, 19-25, and 31 are allowed.

Response to Arguments

Applicant's arguments filed 11/27/06 have been fully considered but they are not persuasive. Applicant argues that Cooper does not disclose "generating performance state data." Examiner disagrees. Applicant and Examiner both agree that Cooper discloses copying default performance state table data when no match is found. The default performance state table data must have been generated at some point in time. Also, the default performance state data is not a random set of data. Inherently, the default performance state table data was specifically generated so one could be reasonably sure that it would be compatible with the processors that make use of the data. Otherwise the invention would not work. Therefore Cooper does disclose generating the default performance state data.

The rejections to claims 7, 12-17, 26-29 and 32 are respectfully maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Yanchus
February 19, 2007